REMARKS

In the Office Action, the Examiner noted that claims 1-22 are pending in the application and that claims 1-22 are rejected. By this response, claims 1, 5, 6, 11, 16 and 20 have been amended to more clearly define the Applicants' invention and not in response to prior art. All other claims continue unamended by this response.

In view of the amendments presented above and the following discussion, the Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, the Applicants believe that all of these claims are now in allowable form.

Rejections

A. 35 U.S.C. § 102

The Examiner has rejected claims 1, 3-9, 11-14, and 16-22 under 35 U.S.C. § 102 as being anticipated by Sharony et al (U.S. Patent No. 5,495,356, hereinafter "Sharony"). The rejection is respectfully traversed.

Claims 1, 5, 6, 11, 16 and 20-22

The Examiner alleges that regarding claims 1 and 5, Sharony discloses in Fig. 3, a generalized switching network, wherein data, arranged as time slots and space connections are received at the nx1 blocks. The Examiner further alleges that Sharony discloses that a system in which an input and/or all inputs are connected to a passive broadcast medium that broadcasts an input and/or all inputs to each one or all of N outputs.

In addition, the Examiner alleges that regarding claims , 11, 16 and 20-22, Sharony discloses a generalized switching network, wherein a plurality of selection blocks are configured to broadcast data from one or more input channels to one or more output channels as a function of space dimension,

wavelength dimension, and time slot dimension. The Examiner urther alleges that Sharony discloses a generalized switching network, wherei data, arranged as time slots and space connections are received at the nxln bl cks and a system in which an input and/or N inputs are connected to a pa sive broadcast medium that broadcasts an input and/or all the inputs to each o e of the N outputs.

As such, the Examiner alleges that Sharony teaches all f the aspects of the Applicants' claims 1, 5, 6, 11, 16 and 20-22. The Applicant respectfully disagree.

The Applicants respectfully submit that Sharony does no teach all of the aspects of the Applicants' invention, at least with respect the A plicants' amended, independent claim 1, which specifically recites:

> "Apparatus for switching data from any of a plura ity of inputs to any of a plurality of outputs, said data formatted as data b ocks containing a fixed number of bits of data, each data block compri ing "O" bit packs containing a number of bits "P", where O and P re integers, said apparatus comprising:
>
> apparatus for receiving a plurality of respecti e input bit packs organized in a combination of input data rails and time s ots,
>
> apparatus for selecting any of the respective in ut bit packs from any of the rails in any of the time slots, and
>
> apparatus for conveying said selected bit pack to any output data position within a combination of output data rails and time slots." (emphasis added).

"Anticipation requires the presence in a single prior art r ference disclosure of each and every element of the claimed invention, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist . Derrick Co., 730 F.2d 1452, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984) (citing Con ell v. Sears, Roebuck & Co., 722 F.2d 1542, 220 U.S.P.Q. 193 (Fed. Cir. 1 83)) (emphasis added).

The Sharony reference fails to disclose each and every element of the claimed invention, as arranged in the claim. The Applicants r spectfully submit that there is absolutely no teaching, suggestion or disclosure i Sharony for at

least an "apparatus for receiving a plurality of respective input b· packs organized in a combination of input data rails and time slots" or ·or an "apparatus for selecting any of the respective input bit packs from any of thi: rails in any of the time slots" as taught in the Applicants' specification and clai ıed by at least the Applicants' claim 1. The Applicants' invention is directed, a least in part, to a switch that receives respective bit packs (i.e., respective bit one:, twos, threes, fours, fives, six, sevens, and eights) of the input data and switcl ıes the respective bit pack " to any output data position within a combination of ou· ɔut data rails and time slots."

In support of at least claim 1, the Applicants, in the specification, specifically recite:

> "In accordance with the principles of the illustrative embodiment, when the switch module 130 receives a data block, e.g. a byte, the disassembler 140 slices the data block into bit-pacl:s, e.g. bits, and distributes the bits to the various switching cores 150-1:8. Consequently, all the respective bit ones, twos, threes, fours, fives, six, sevens, and eights from data channels input to the disassembler 1·) are respectively routed to the switching core 150, 152, 154, 156, . . . 158." (See Specification page 7, lines 13-18).
>
> "Within each switching core 150-158 all the rel·vant bits (e.g., bit 1's for switch module 130, bit 2's for switch mo·.ule132, etc.) are illustratively input to the switching core on 16 rails in ·18 time slots (note that 16x48=768). Each rail is carrying data at the rate ·.f 311.04 Mb/s. In this manner, the data rate of 768 STS-1 signals can be accommodated by 8 such devices. That is, since the transmission rate of an STS-1 signal is 51.84 megabits per second (Mbps), 768 such sign:ls would yield a transmission rate of 39.81 Gigabits per second (Gbp s). Because each device's switching core operates on one bit of each of t e 768 channels in parallel, with each bit being processed at a rate of (number of rails per switching core) X (number of switching cores)X(switch processing speed) = 16 X 8 X 311.04 Mbps = 39.81 Gbps, the data ate of 768 STS-1 signals." (See Specification page 11, lines 8-17).

As evident from at least the excerpts of the Applicants' ·pecification recited above, the Applicants' invention is directed, at least in ·art, to advantageously perform switching on respective individual pit :acks of an input data signal in parallel.

Sharony teaches a switching network that utilizes at leas three degrees of freedom, time, wavelength and space. In one embodiment of Sharony, each space channel between an input and an output is assigned a time slot and wavelength coordinate characteristic of the output and the input transmitter and output receiver are tuned to the appropriate time and wavelength coordinates and selective switching is used to complete the space channel between the input and output. In another embodiment of Sharony, each input channel is assigned a set of space, time slot and wavelength coordinates and an input signal is broadcast to all of the outputs which selectively makes connection to those inputs with an appropriate set of coordinates. (See Sharony, Abstract). In contrast to the Applicants' invention, however Sharony specifically teaches:

> "The STSW has two stages, the first stage shown in FIG. 3 is composed basically of n mxm star couplers 31 and the second stage shown is composed of m nxln Wavelength-Time Selective Switches 32 (WTSSs). The two stages are connected to each other by mn optical links 33, that may be optical fibers. To each one of the n star couplers 31, m optical transmitters 34 are connected, each fixed with a different wavelength (e.g., .lambda..sub.0, .lambda..sub.1, . . . ambda..sub.m-1). Each optical transmitter 34 is driven by an electrical signal composed of l inputs multiplexed in time (e.g., t.sub.0,t.sub.1, . . . t sub.l-1) by a time division multiplexer 35. Thus, each input channel space is uniquely identified by a triplet indicating the fixed sub-channels it uses in each of the three dimensions, i.e., (s.sub.i, .lambda..sub.j, t.sub.p). Each WTSS 32 has In outputs and it receives the entire information from all the N inputs." (See Sharony, col. 5, lines 46-60). (emphasis added).

In the invention of Sharony, each of the WTSS receives the entire information from all the N inputs. The invention of Sharony does not, and further, is not capable of performing the switching taught and claimed by the Applicants' invention. More specifically, the invention of Sharony does not teach, suggest or disclose a switch comprising an "apparatus for receiving a plurality of respective input bit packs organized in a combination of input data rails and time slots" or for an "apparatus for selecting any of the respective input bit packs from any of the rails in any of the time slots" as taught in the Applicants' specification and

claimed by at least the Applicants' claim 1. The invention of Sharony does not teach performing the switching of data separated into bit packs wherein the bit packs are respectively switched (i.e., each bit pack is switched in parallel by a respective switch.) As such, and for at least the reasons stated herein, the Applicants respectfully submit that Sharony fails to teach each and every element of the claimed invention, as arranged in the claim, and as such fails to anticipate the invention of the Applicants.

Therefore, the Applicants submit that independent claim 1 is not anticipated by the teachings of Sharony and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claims 5, 6, 11, 16 and 20 recite similar relevant features as recited in independent claim 1. As such, the Applicants submit that independent claims 5, 6, 11, 16 and 20 are also not anticipated by the teachings of Sharony and also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

Furthermore, dependent claims 3-4, 7-9, 12-14, 17-19 and 21-22 depend either directly or indirectly from independent claims 1, 6, 11, 16 and 20 and recite additional features therefor. As such and for at least the reasons set forth herein, the Applicants submit that dependent claims 3-4, 7-9, 12-14, 17-19 and 21-22 are also not anticipated by the teachings of Sharony. Therefore the Applicants submit that dependent claims 3-4, 7-9, 12-14, 17-19 and 21-22 also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

The Applicants reserve the right to establish the patentability of each of the claims independently in subsequent prosecution.

B. 35 U.S.C. §103

The Examiner rejected claim 2 under 35 U.S.C. §103(a) as being unpatentable over Sharony in view of Sheafor et al. (U.S. Patent No. 6,223,242, hereinafter "Sheafor"). The rejection is respectfully traversed.

Claim 2 depends directly from independent claim 1 and recites additional features therefor. The Examiner applied Sharony for the rejection of the Applicants' claim 2 as described above for the rejection of the Applicants' independent claim 1. The Applicants respectfully submit that for at least the reasons disclosed above, the teachings of Sharony do not teach, suggest, or otherwise render obvious the Applicants' invention, at least with regard to the Applicants' independent claim 1. Therefore the Applicants submit that at least because Sharony does not teach, suggest, or describe the invention of the Applicants regarding at least claim 1, the teachings of Sharony also do not teach, suggest, or describe the Applicants' claim 2, which depends from independent claim 1 and as such, do not anticipate or render the Applicants' claim 2 obvious.

The Examiner correctly concedes that Sharony does not teach or disclose that each bit pack is one bit wide. As such the Examiner cites Sheafor for teaching that each bit pack is one bit wide. The Examiner further alleges that it would have been obvious to one having ordinary skill in the art to configure each bit pack as one bit in Sharony's system as suggested by Sheafor.

It should be noted, however, that the teachings of Sheafor, alone, also do not teach, suggest, or describe the invention of the Applicants. at least with respect to independent claim 1. The Sheafor reference teaches a crossbar routing arrangement for use in a digital system having three or more buses. An associated method is also disclosed. The routing arrangement is configured for transferring a set of data received from any particular one of the buses to any other selected one of the buses and includes a control arrangement associated with each bus for dividing the set of data into at least first and second subsets of data and for adding self-routing signals to each data subset which signals identify the selected bus. (See Sheafor, Abstract). It is clear, however, that the teachings of Sheafor, alone, also do not render obvious the Applicants' invention, at least with respect to claim 1 and an "apparatus for receiving a plurality of respective input bit packs organized in a combination of input data rails and time

slots" or for an "apparatus for selecting any of the respective input bit packs from any of the rails in any of the time slots".

Furthermore, the Applicants submit that there is absolutely no suggestion or motivation in any of the references to combine the teachings of Sharony and Sheafor as suggested by the Examiner.

For prior art reference to be combined to render obvious a subsequent invention under 35 U.S.C. § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. Uniroyal v. Rudkin-Wiley, 5 U.S.P.SQ.2d 1434, 1438 (Fed. Cir. 1988). The teachings of the references can be combined only if there is some suggestion or incentive in the prior art to do so. In re Fine, 5 U.S.P.SQ.2d 1596, 1599 (Fed. Cir. 1988). Hindsight is strictly forbidden. It is impermissible to use the claims as a framework to pick and choose among individual references to recreate the claimed invention Id. at 1600; W.L. Gore Associates, Inc., v. Garlock, Inc., 220 U.S.P.Q. 303, 312 (Fed. Cir. 1983).

Moreover, the mere fact that a prior art structure could be modified to produce the claimed invention would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

The Applicants further submit that even if a suggestion to combine the references as suggested by the Examiner did exist (which the Applicants submit that no such suggestion exists), the Examiner's attention is directed to the fact that the alleged references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious the Applicants' invention, at least with regard to the Applicants' independent claim 1. The substantial gap between the teachings of Sharony and the invention of the Applicants is not bridged by the teachings of Sheafor. The combination of the teachings of Sharony and Sheafor fail to teach at least an "apparatus for receiving a plurality of respective input bit packs organized in a combination of input data rails and time slots" or for an

"apparatus for selecting any of the respective input bit packs from any of the rails in any of the time slots" as taught in the Applicants' specification and claimed by at least the Applicants' claim 1. Therefore, at least because the teachings of Sharony and Sheafor, alone or in any allowable combination, do not teach, suggest or disclose the Applicants' claim 1, the Applicants further submit that the teachings of Sharony and Sheafor, alone or in any allowable combination, also do not teach, suggest or disclose the Applicants' claim 2, which depends directly from the Applicants' independent claim 1.

Therefore, the Applicants respectfully submit that claim 2 as it now stands, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

The Applicants reserve the right to establish the patentability of each of the claims independently in subsequent prosecution.

C. 35 U.S.C. §103

The Examiner rejected claims 10 and 15 under 35 U.S.C. §103(a) as being unpatentable over Sharony. The rejection is respectfully traversed.

Claims 10 and 15 depend directly from independent claims 6 and 11, respectively, and recite additional features therefor. The Examiner applied Sharony for the rejection of the Applicants' claims 10 and 15 as described above for the rejection of the Applicants' independent claims 6 and 11. The Applicants respectfully submit that for at least the reasons disclosed above, the teachings of Sharony do not teach, suggest, or otherwise render obvious the Applicants' invention, at least with regard to the Applicants' independent claims 6 and 11. Therefore the Applicants submit that at least because Sharony does not teach, suggest, or describe the invention of the Applicants regarding at least claims 6 and 11, the teachings of Sharony also do not teach, suggest, or describe the Applicants' claims 10 and 15, which depend from independent claims 6 and 11 and as such, do not anticipate or render the Applicants' claims 10 and 15 obvious.

Therefore, the Applicants respectfully submit that claims 10 and 15, as they now stand, fully satisfy the requirements of 35 U.S.C. § 10 and are patentable thereunder.

The Applicants reserve the right to establish the patentability of each of the claims independently in subsequent prosecution.

Conclusion

Thus, the Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. § 103. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Jorge Tony Villabon, Esq. at (732) 530-9404 x1131 or Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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